

Pspice Simulation of Hysteretic Current Mode Control Inverter

While reading different articles on DCAC inverter design, I decided to create a Pspice modeling and simulation of a hysteretic current mode controller. I could not find any Pspice model of ACDC inverter on internet There are a lot of the made in MATLAB Simulink. MATLAB is behavior modeling so I decided to apply Pspice behavior modeling as well.

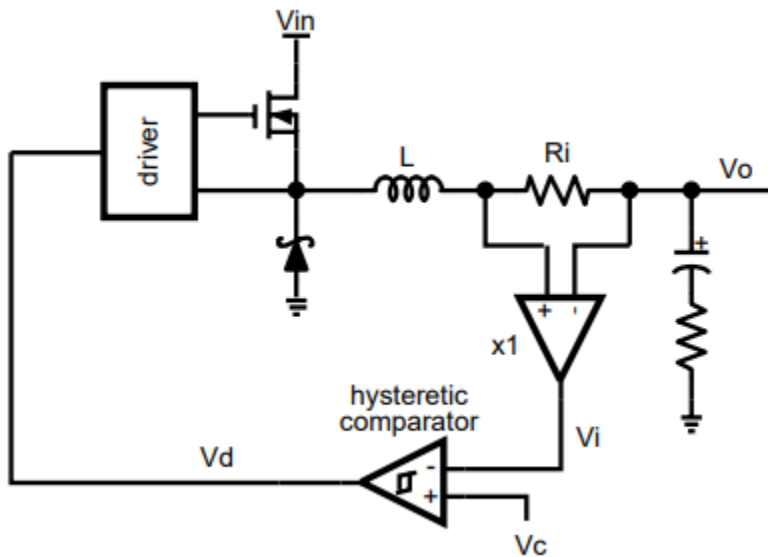
Below is simplified schematic of Hysteretic Mode Buck Current Regulator from an TI article.

Every time the error between control references and control variables crosses either the positive or negative hysteresis band's boundary, a significant change in the controller's output.

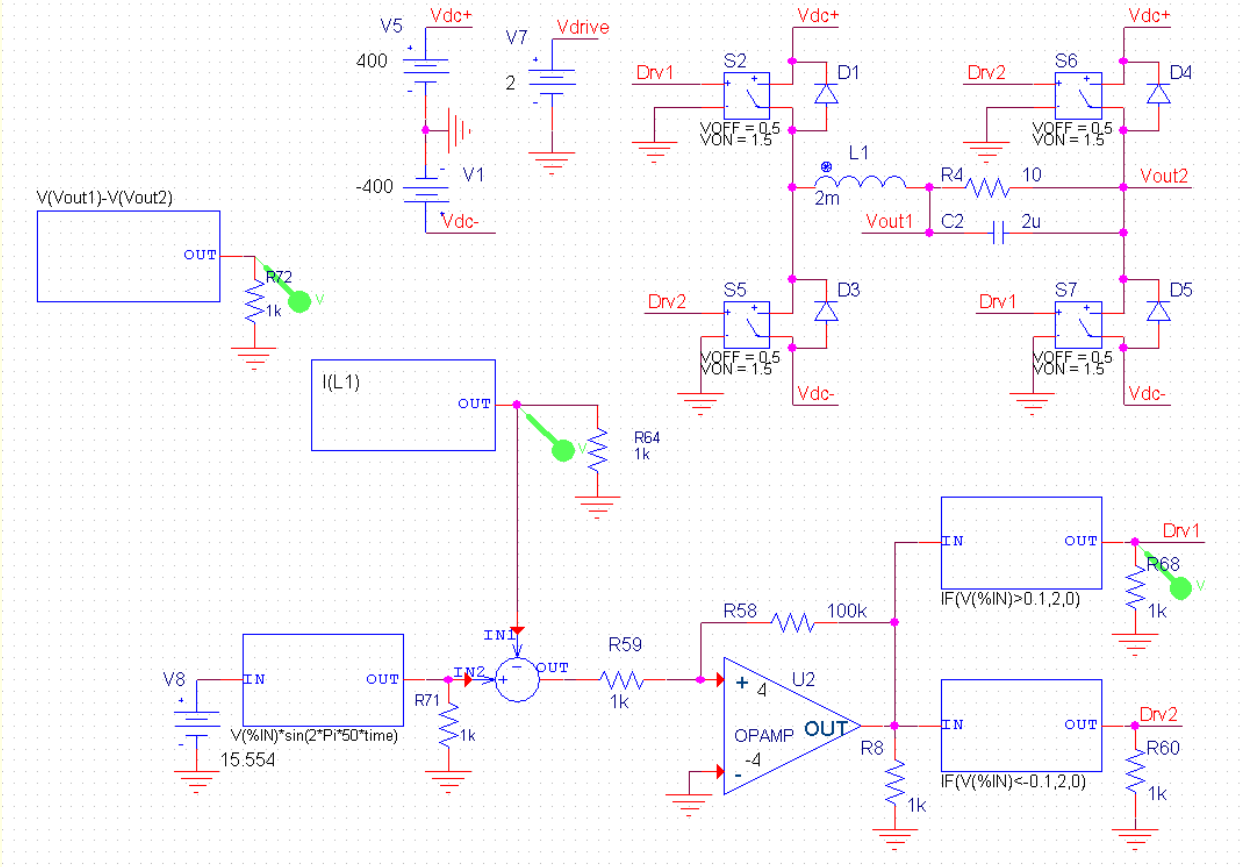
Thus the controller quickly reacts to any deviation from control references, which are the reason of the high gain behavior of these controllers.

Interesting is that there is no hysteretic boundaries present on the schematic below. Hysteretic deviations are determined by amplification/ response time of feedback loop.

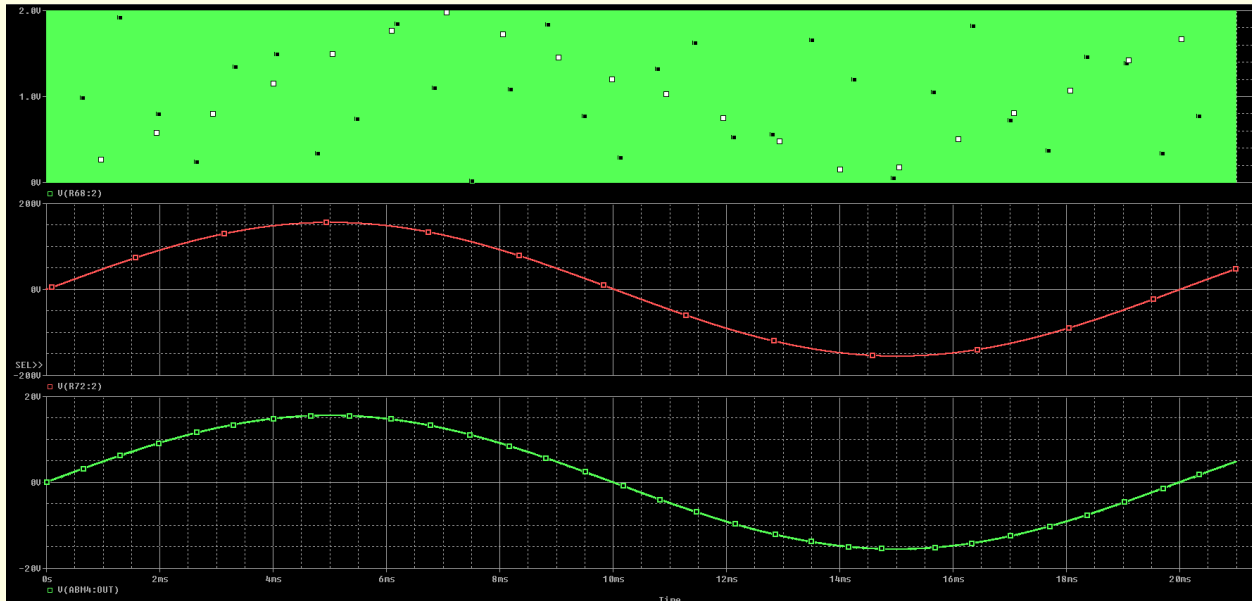
Hysteretic Mode Buck Current Regulator



Pspice modeling of Hysteretic Current Mode Current Regulator/ Inverter



Simulation Results

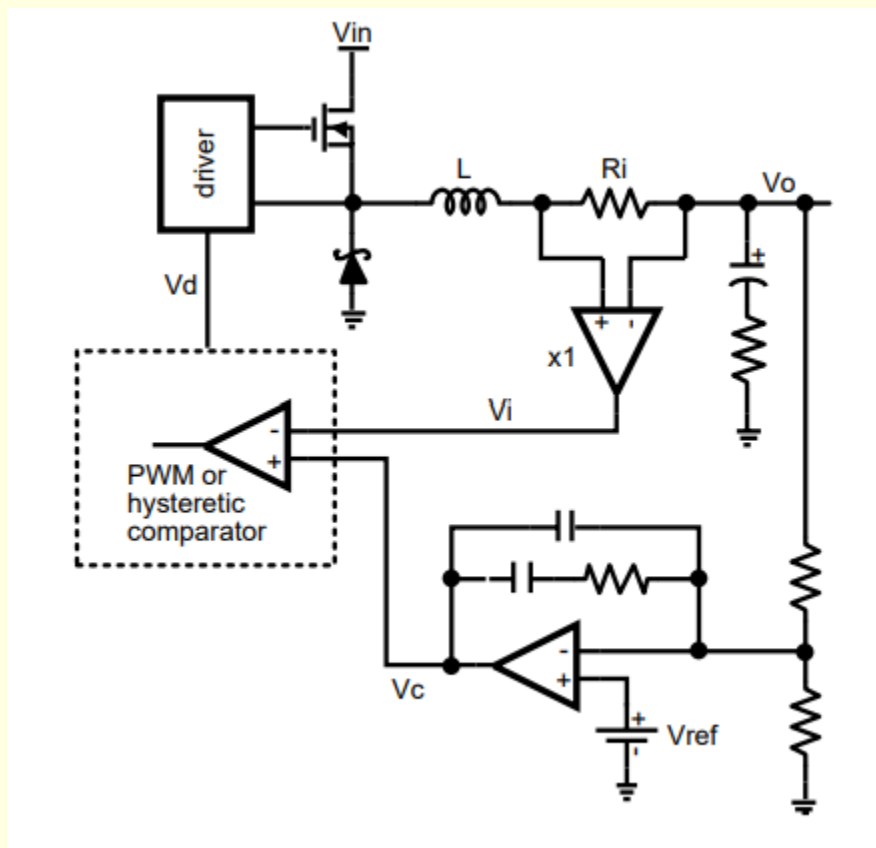


As you can see from the second graph, the switching frequency is high, about 2.5MHz. Current hysteresis window is small, about $\pm 0.25v$.

Current Mode Hysteretic Buck Converter

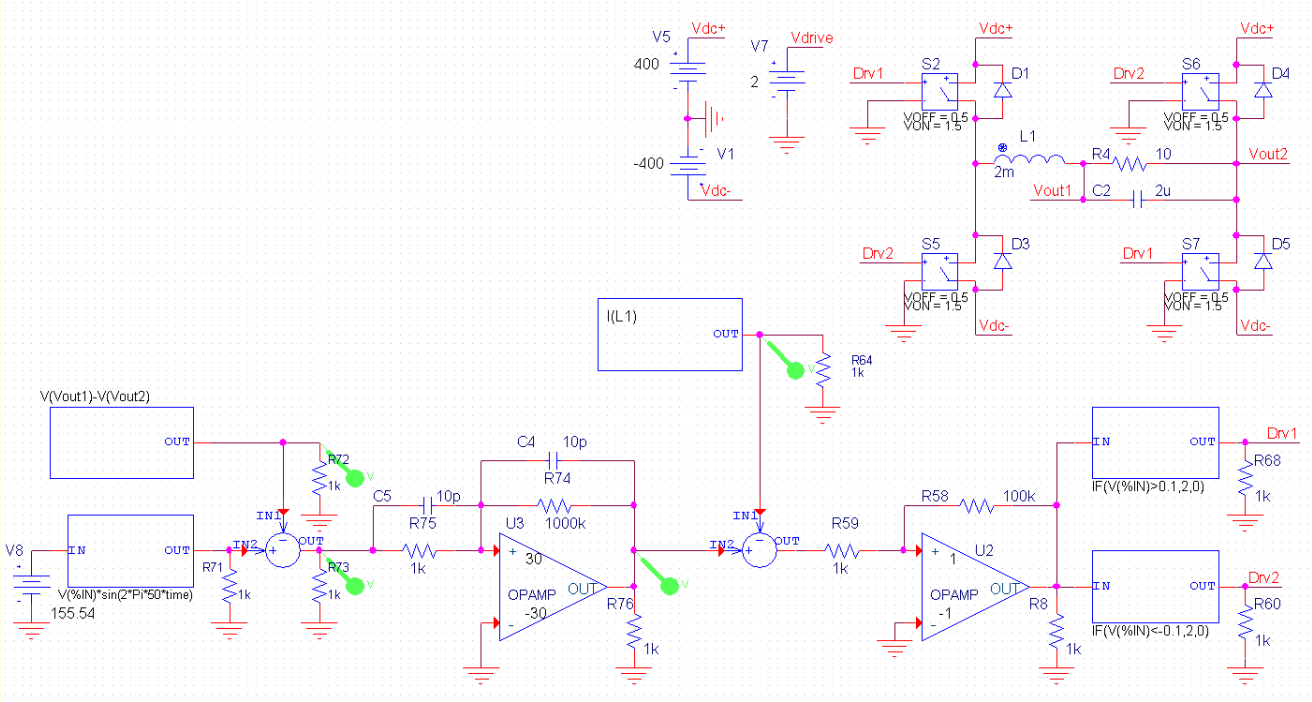
Now on the next drawing you see current mode hysteretic buck voltage regulator. It is based on the previous hysteretic current regulator with addition of an external voltage loop. Again, there is no hysteretic boundaries present.

To construct the circuit as a voltage regulator, the control voltage V_c should respond in some manner to the error voltage (difference between the properly ratioed output voltage and the reference voltage) so that inductor current is continuously adjusted to keep the output voltage regulated.

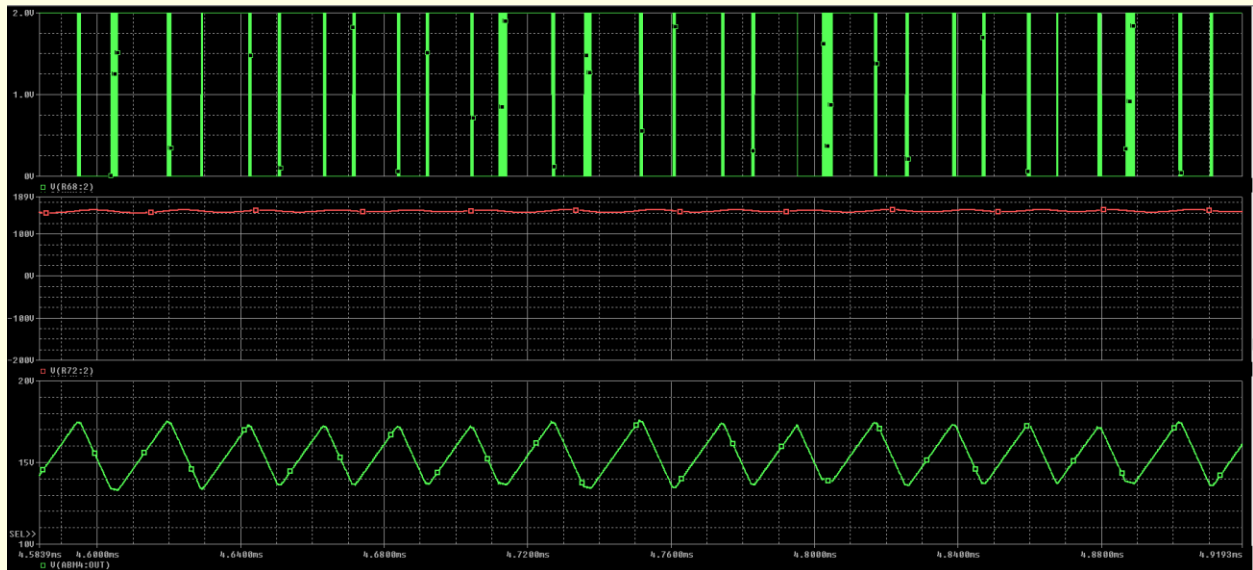
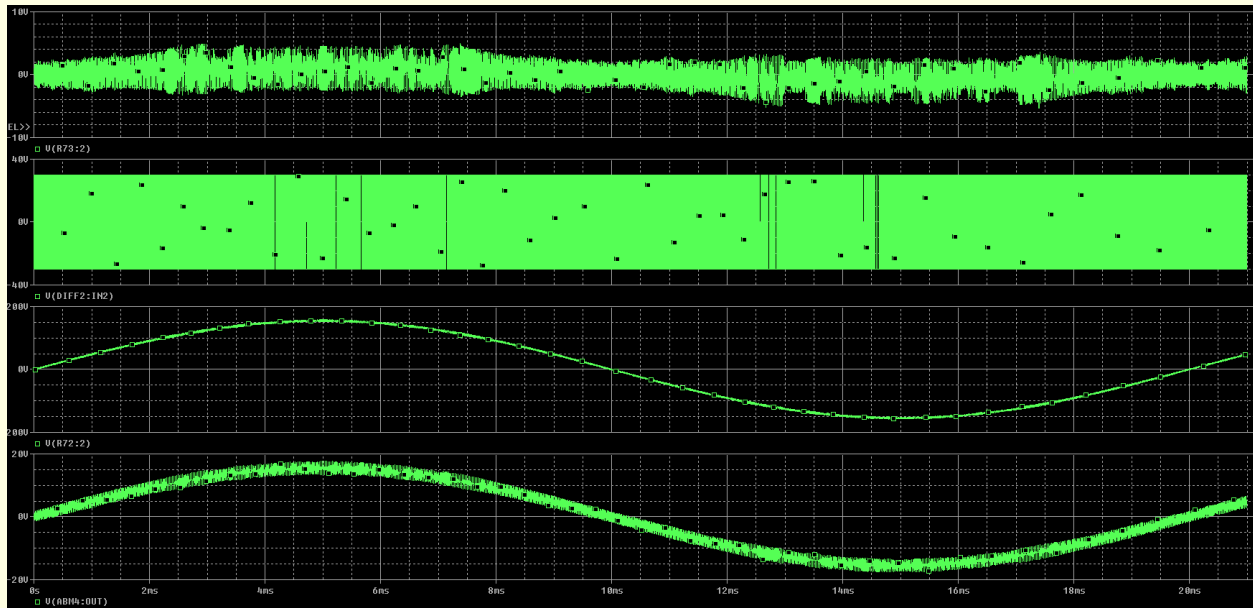


Pspice modeling of Hysteretic Current Mode Control Inverter – Version 1

The schematic below is built similar to the schematic of buck voltage regulator from TI article shown on previous page. As you can see, there is no hysteretic boundaries, just comparator.



Simulation Results

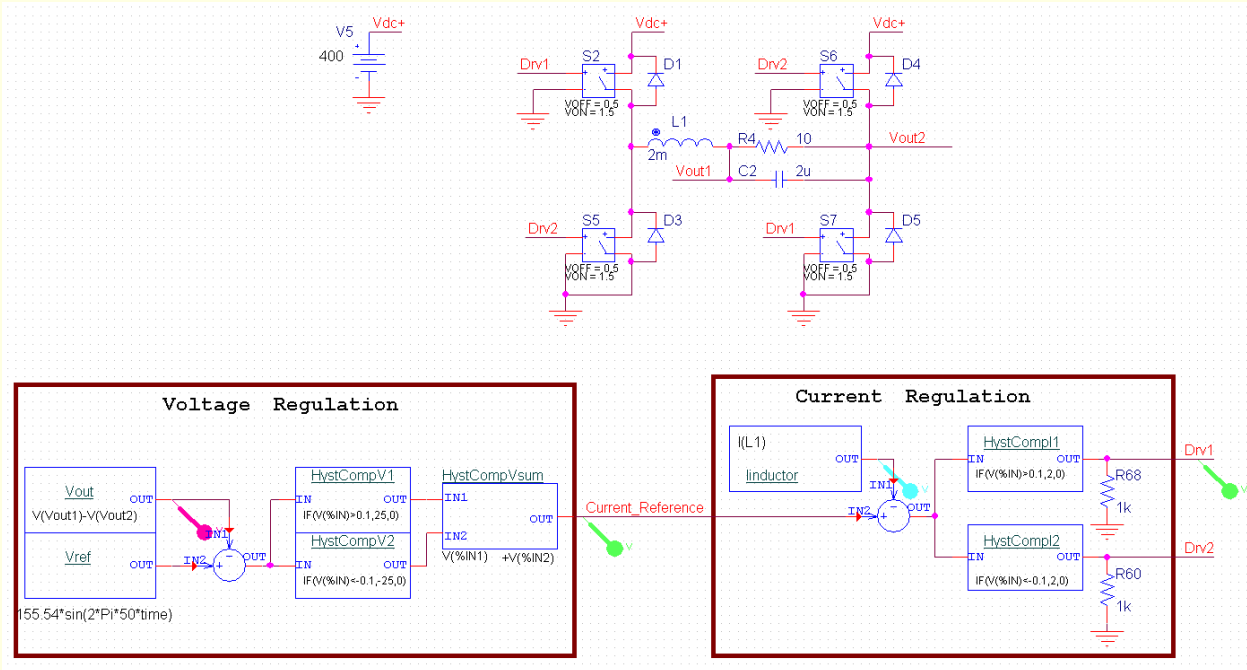


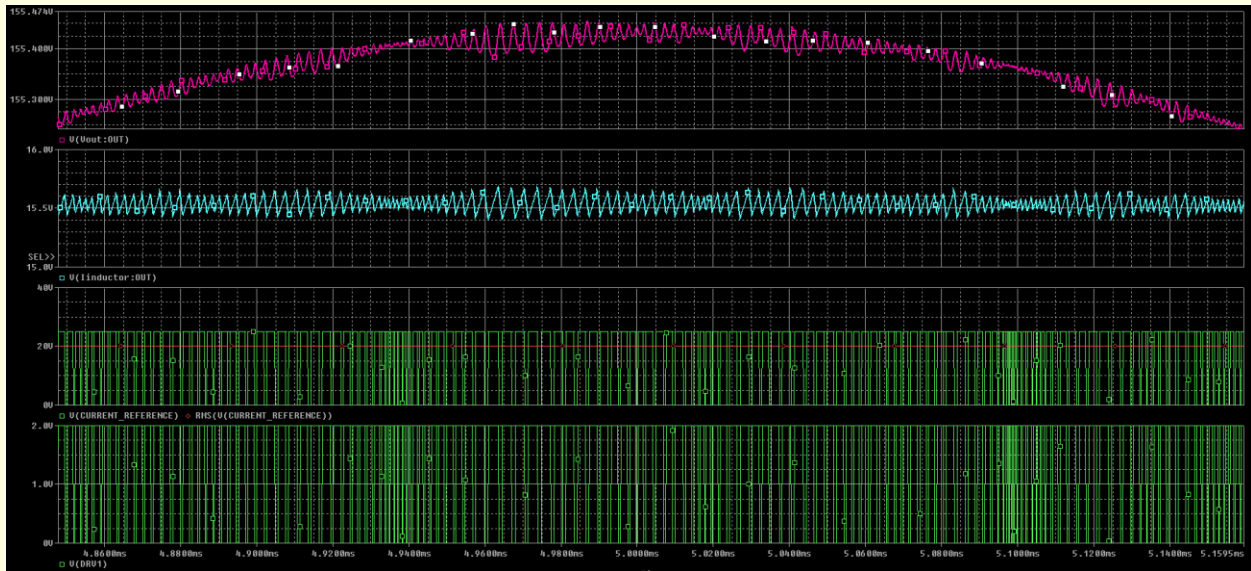
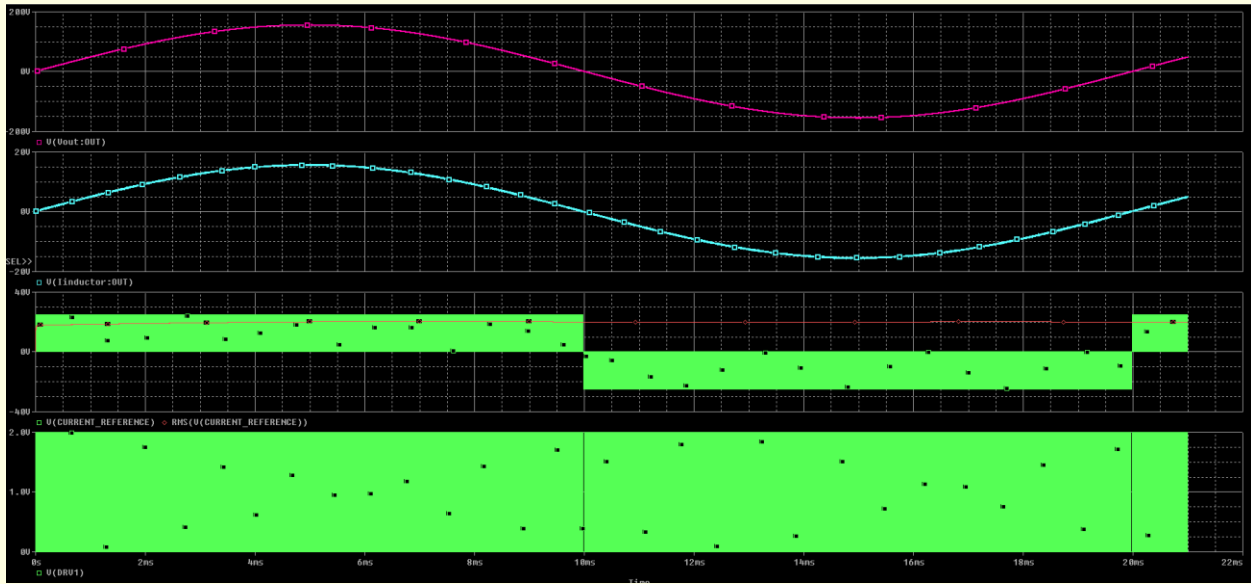
It appears that hysteretic output voltage and inductor current ripples became quite large and switching frequency went down considerably, to roughly 50 kHz, see oscillograms above.

This slow response is most probably caused by output capacitor C2 and finite gain of voltage error amplifier.

Pspice modeling of Hysteretic Current Mode Control Inverter – Version 2

In an effort to improve the characteristics of the inverter model I decided to replace external voltage loop error amplifier with hysteretic comparators. The comparators have hysteresis limits which can be reduced to low values, speeding up the reaction time. In our case I made the hysteresis limits equal to 0.1v.





As you can see from the simulation graphs above, the quality of the output signal is improved dramatically. Output voltage ripple value is contained within $\pm 0.1\text{V}$ hysteresis window.

Ripple current value also diminished to somewhere $\pm 0.1\text{A}$.

The hysteretic switching frequency is about 300 kHz.

Interesting consequence of this change of the feedback control circuit is that the inverter became unipolar, as one can see from the first graph.